# CHAPTER EIGHT

Schottky Transistor-Transistor logic (STTL)

Digital flectronics.

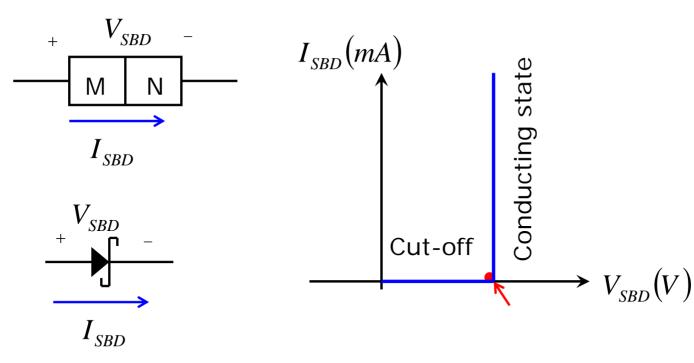
Schottky Transistor-Transistor
Logic (STTL)

STTL is obtained by replacing the BJT with Schottky-clamped BJT (SBJT)

The primary advantage of SBJTs is their improved transient times since SBJT do NOT operate in saturation

# Schottky-Barrier Diodes (SBD)

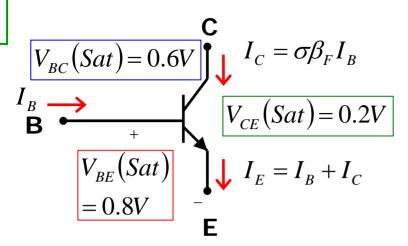
Schottky-barrier diode is made by adjoining **m**etal and **N**-type semiconductor (usually aluminum with N-type silicon)



Circuit symbol

Current voltage characteristics

## Schottky-Clamped SBJT



**Saturation Mode** 

The saturation can be <u>avoided</u> by limiting the forward-biased base-collector voltage to values <u>less</u> than 0.6 V

A serious problem that <u>limits</u> the switching speed of a BJT inverter as well the TTL gates is the time required to <u>remove</u> the enormous <u>stored charge</u> of the base of a <u>saturated BJT</u>.

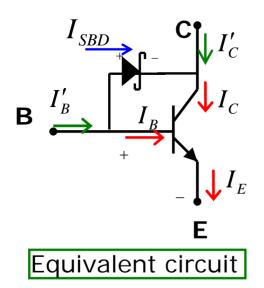
Thus, the solution is to use BJTs that do not saturate.

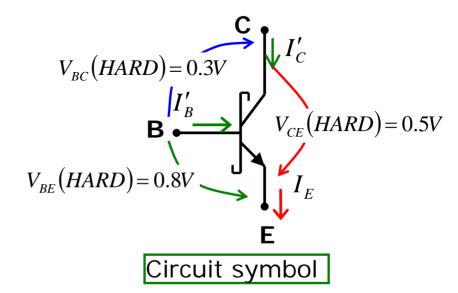
The saturation mode is characterized by the forward biased B-C voltage

$$V_{BC}(sat) = V_{BE}(sat) - V_{CE}(sat)$$
  
= 0.8 - 0.2 = 0.6V

This is accomplished by placing SBD across the base and collector terminals of a BJT.

## Schottky-Clamped SBJT





 $V_{BC}$  is limited to  $V_{SBD}(ON) = V_{BC}(HARD) = 0.3V$ 

#### The 'ON-HARD' Mode:

- 1. BJT is F.A.
- 2. Schottky diode is conducting

The SBJT does not saturate



 $\sigma = 1$ 

## Schottky-Clamped SBJT

#### "Inverse-active" Schottky Mode:

Since  $V_{BC}$  is limited to  $V_{SBD}(ON) = V_{BC}(HARD) = 0.3V$  $V_{BC}(RA) = 0.7V$ 

The SBJT can not operate in inverse active mode

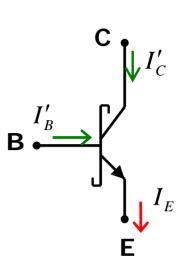
#### However, for

$$V_{BE} < V_{BE}(FA), \ V_{BC} = V_{BC}(RS) = 0.3V$$

$$I_C' = -I_{SBD}$$

$$I_B' = I_{SBD}$$

$$I_B = I_C = I_E = 0$$



# Schottky-Clamped SB.

= 0.5V



Determine the logic swing of SBJT shown, assuming

### Solution

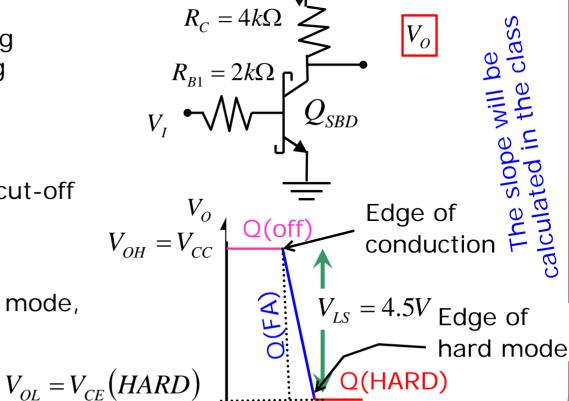
 $\frac{V_{OH}}{V_{OH}}$  When  $V_{I}$  is low, SBJT is cut-off

 $I_{RC} = I_C = 0 \qquad V_{OH} = V_{CC} = 5V$ 

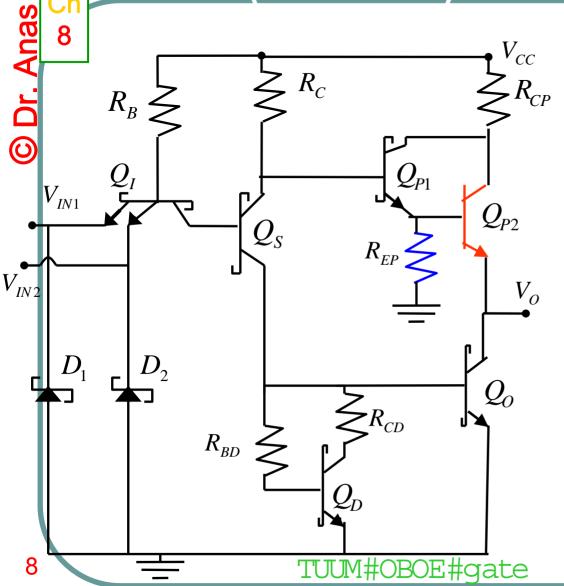
→ SBJT is "ON-HARD" mode,  $V_{OL} = V_{CE}(HARD) = 0.5V$ 

 $=V_{OH}-V_{OL}=4.5V$ 

Logic swing voltage=



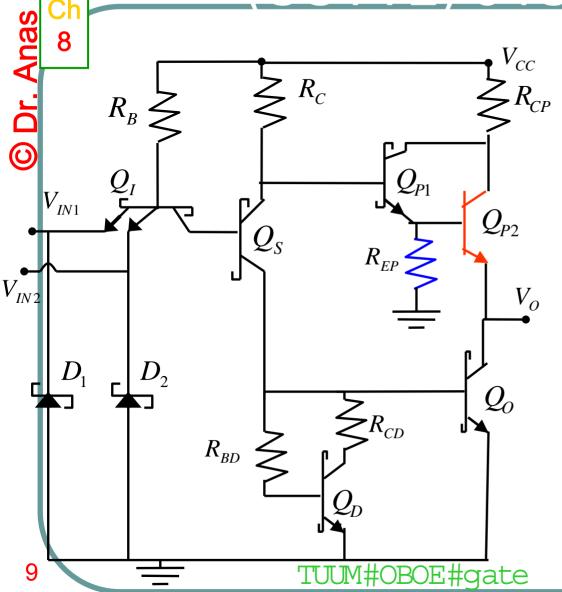
# Schottky-Clamped TTL (SSTTL) 54S00/74S00



- BJTs are replaced with SBJTs  $R_{CP}$  (except for  $\Omega_{P2}$ )
  - •The Darlington pair  $(Q_{P1} \& Q_{P2})$  provides higher current to charge the load capacitance (Output low-high)
  - •Q<sub>P2</sub> is a normal BJT because it can not saturate since

$$V_{CE,P2}(FA) = V_{CE,P1}(HARD) + V_{BE,P2}(FA)$$
$$V_{CE,P2}(FA) > V_{CE}(sat)$$

# Schottky-Clamped TTL (SSTTL) 54S00/74S00

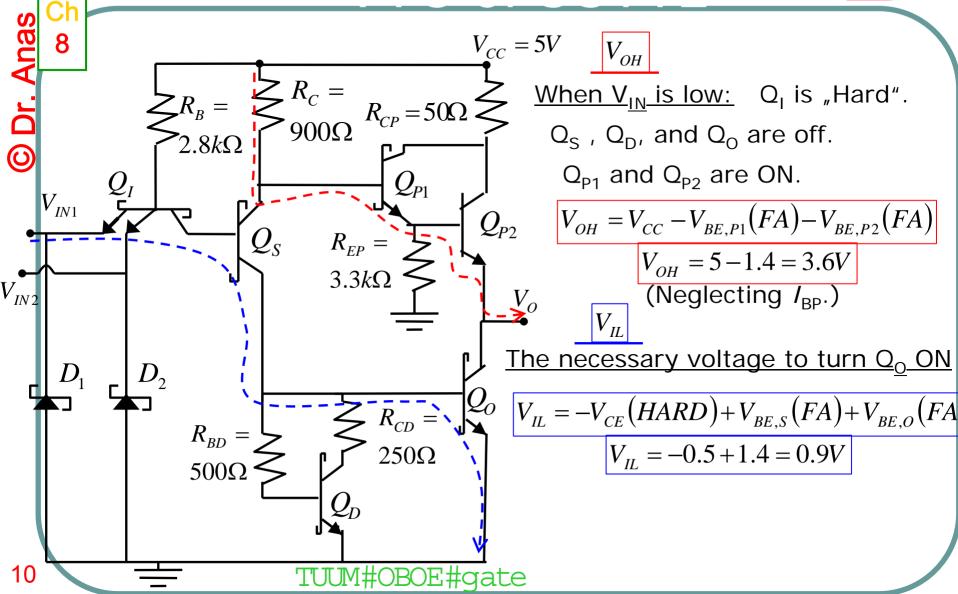


Advantages of  $Q_D$ ,  $R_{BD}$ ,  $R_{CD}$ :

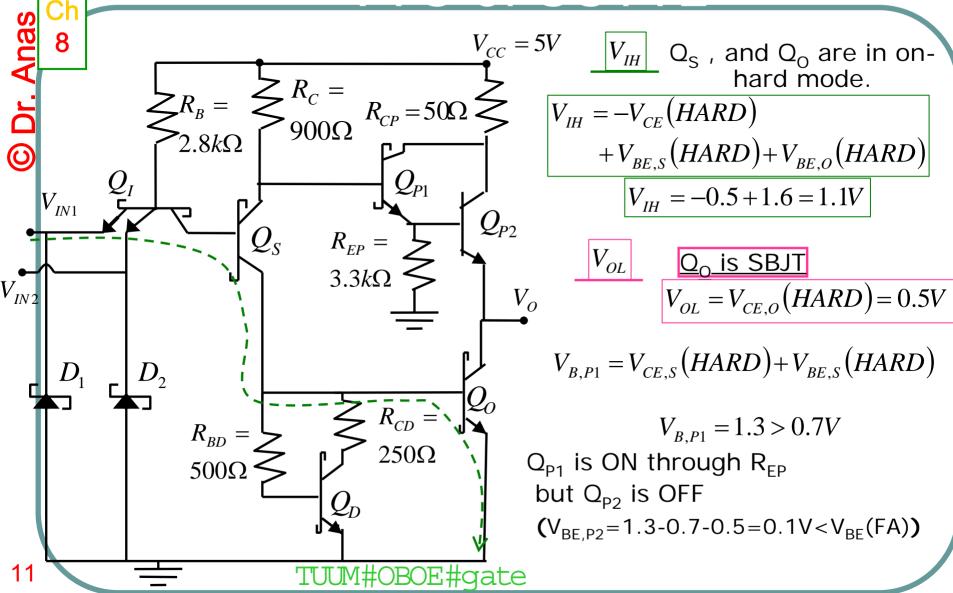
- 1. The break point between  $V_{OH}$  and  $V_{OL}$  is eliminated  $(Q_S, Q_O \text{ turn ON at the same time})$
- Narrower transition width and better noise margin
- 3. Discharge the base charge of  $Q_0$  during the low-high transition

 $R_{B}$ ,  $R_{C}$  have smaller values than in TTL gates to increas the fan-out (but also increase  $P_{CC}(avg)$ )

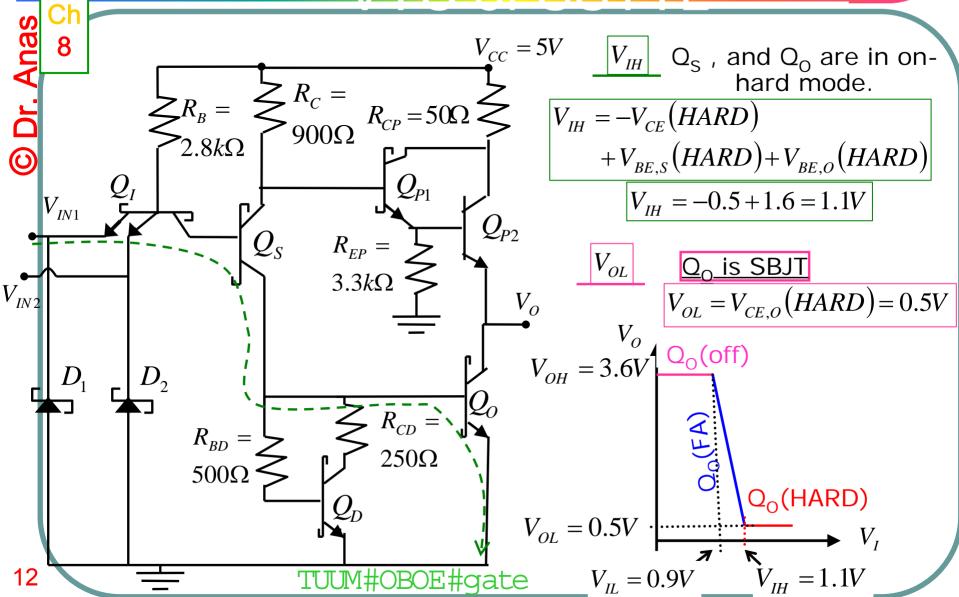
## VTC of SSTTI



### VTC of SSTTI

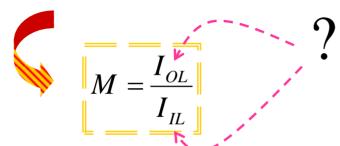


# VTC of SSTTL



### STTL Fan-Out

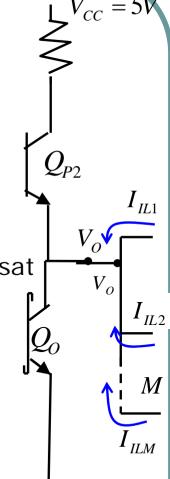
When the output is high,  $I_{IL}$  is negligible. Therefore, Fan-out depends on the output low state



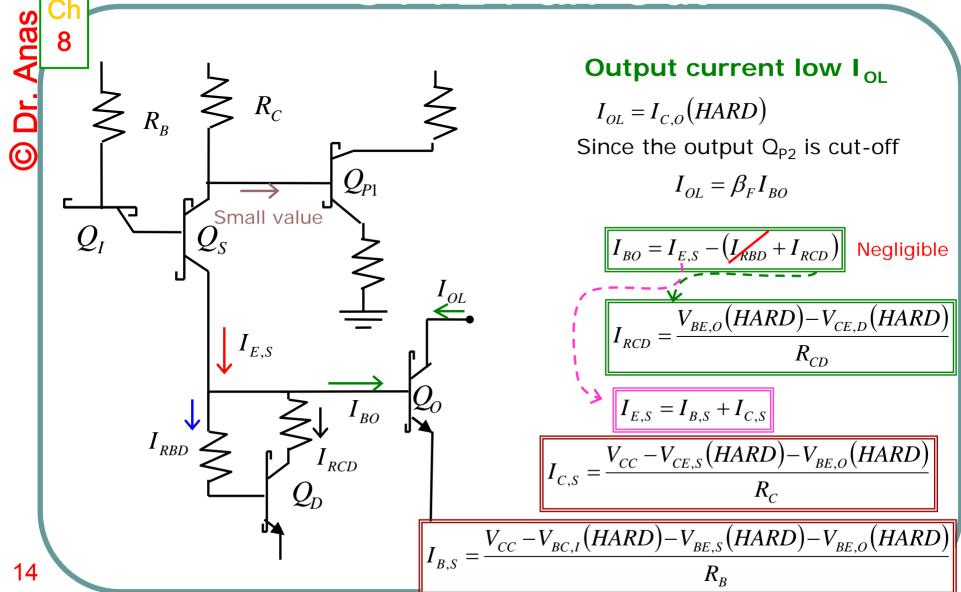
Input current low I<sub>IL</sub>

For the input low state,  $Q_I$  is sat and  $Q_S$  is cut-off

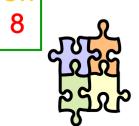
$$I_{IL} = I_{EI} = I_{RB} = \frac{V'_{CC} - V'_{BE,I}(HARD) - V_{CE,O}(HARD)}{R'_{B}}$$



### STTL Fan-Out



## Fan-Out



### Example

Determine the maximum fan-out of the SBJT circuit shown, assuming  $\beta_F = 49$ 

### Solution

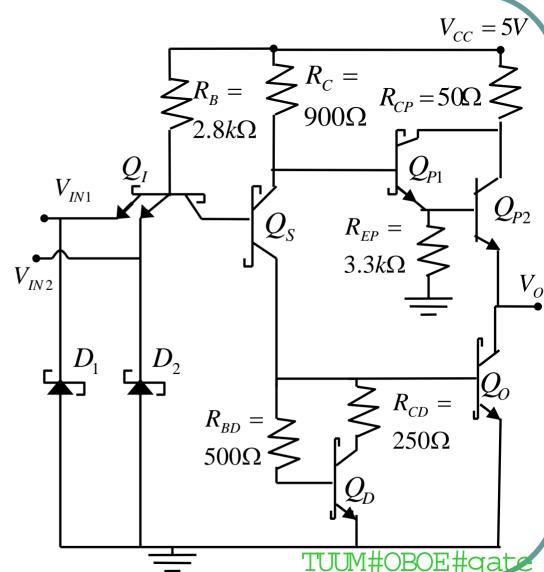
$$I_{IL} = \frac{5 - 0.8 - 0.5}{2.8k} = 1.32mA$$

$$I_{RCD} = 1.2mA$$
  $I_{B,S} = 1.11mA$ 

$$I_{RS} = 1.11 mA$$

$$I_{C,S} = 4.11 mA$$

$$M = 149$$



HW #8:Solve Problems:8.1, 8.3, 8.8,
 and 8.19